

# JAPANESE PATENT OFFICE – Patent Abstracts of Japan

Publication Number: 08204137 A

Date of Publication: 1996.08.09

Int.Class: H01L 27/04

Date of Filing: 1995.01.31

Applicant: MATSUSHITA ELECTRIC IND  
CO LTD

Inventor: HIRANO HIROSHIGE

TANIGUCHI TAKASHI

CHATANI SHIGEO

MORIWAKI NOBUYUKI

NAKANE JOJI

NAKAKUMA TETSUJI

HONDA TOSHIYUKI

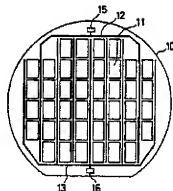
SATOU HISAHIRO

SEMICONDUCTOR DEVICE AND BURN-IN  
METHOD

## Abstract

**PURPOSE:** To enable a semiconductor chip in acceptable wafer state to be burned in even if any defective semiconductor chip happened to be developed simultaneously with the acceptable one.

**CONSTITUTION:** A plurality of semiconductor chips 11 having a power supply voltage line to be impressed with the same as well as an earth voltage line to be impressed with the same are formed on a semiconductor wafer 10. Besides, the first wiring layer 13 for supplying the power supply voltage and the second wiring layer for supplying the earth voltage 12 connected neither to the power supply voltage line nor to the earth voltage line are formed on the semiconductor wafer 10. At this time, the power supply line of semiconductor chip judged to be acceptable by inspection and the first wiring layer 13 as well as the earth voltage line and the second wiring line are respectively connected electrically.



COPYRIGHT: (C)1996.JPO